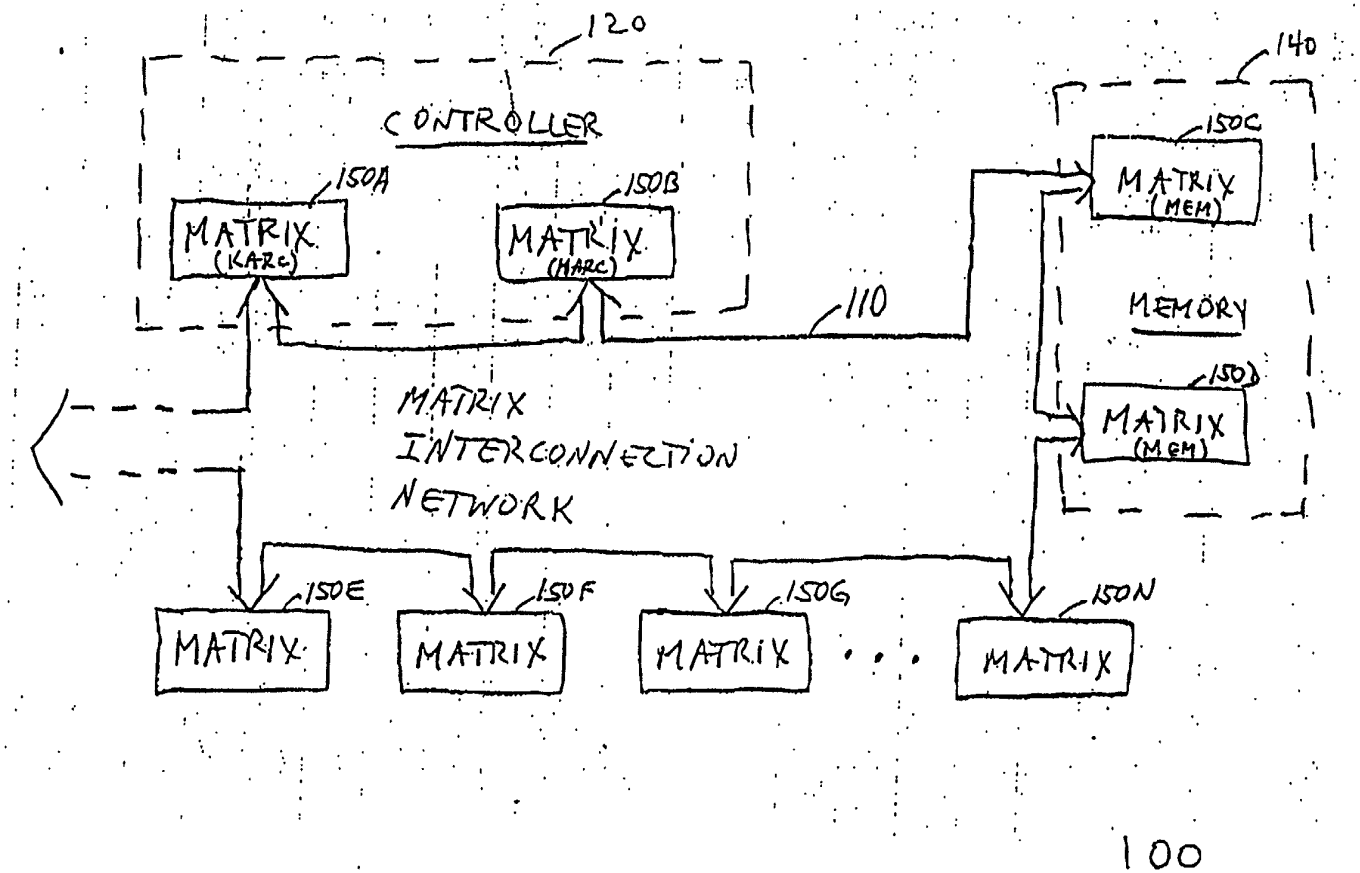


ADAPTIVE COMPUTING ENGINE (ACE)

FIG. 1

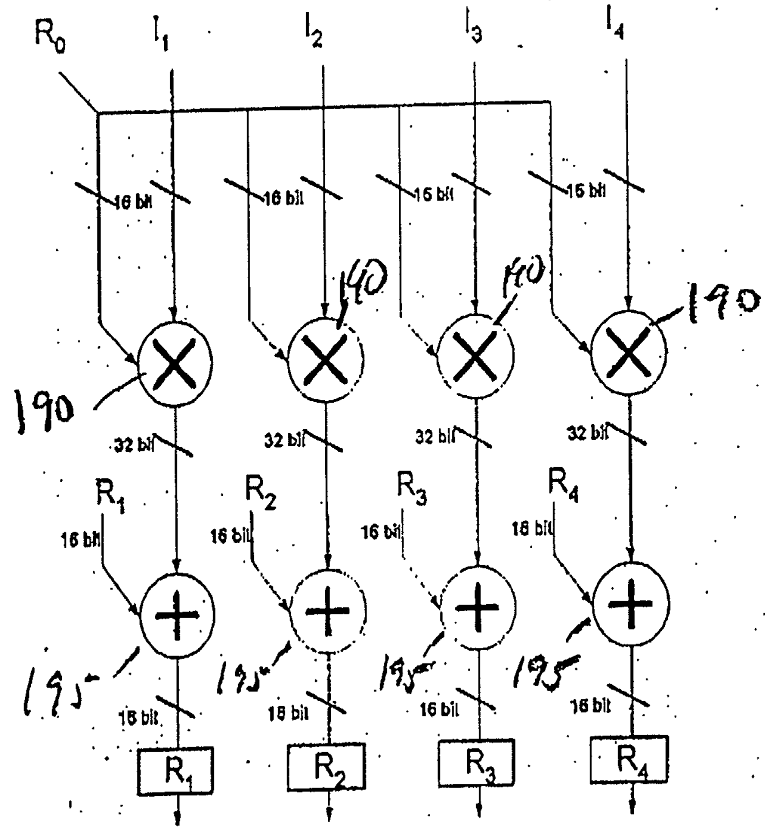


FIG. 2

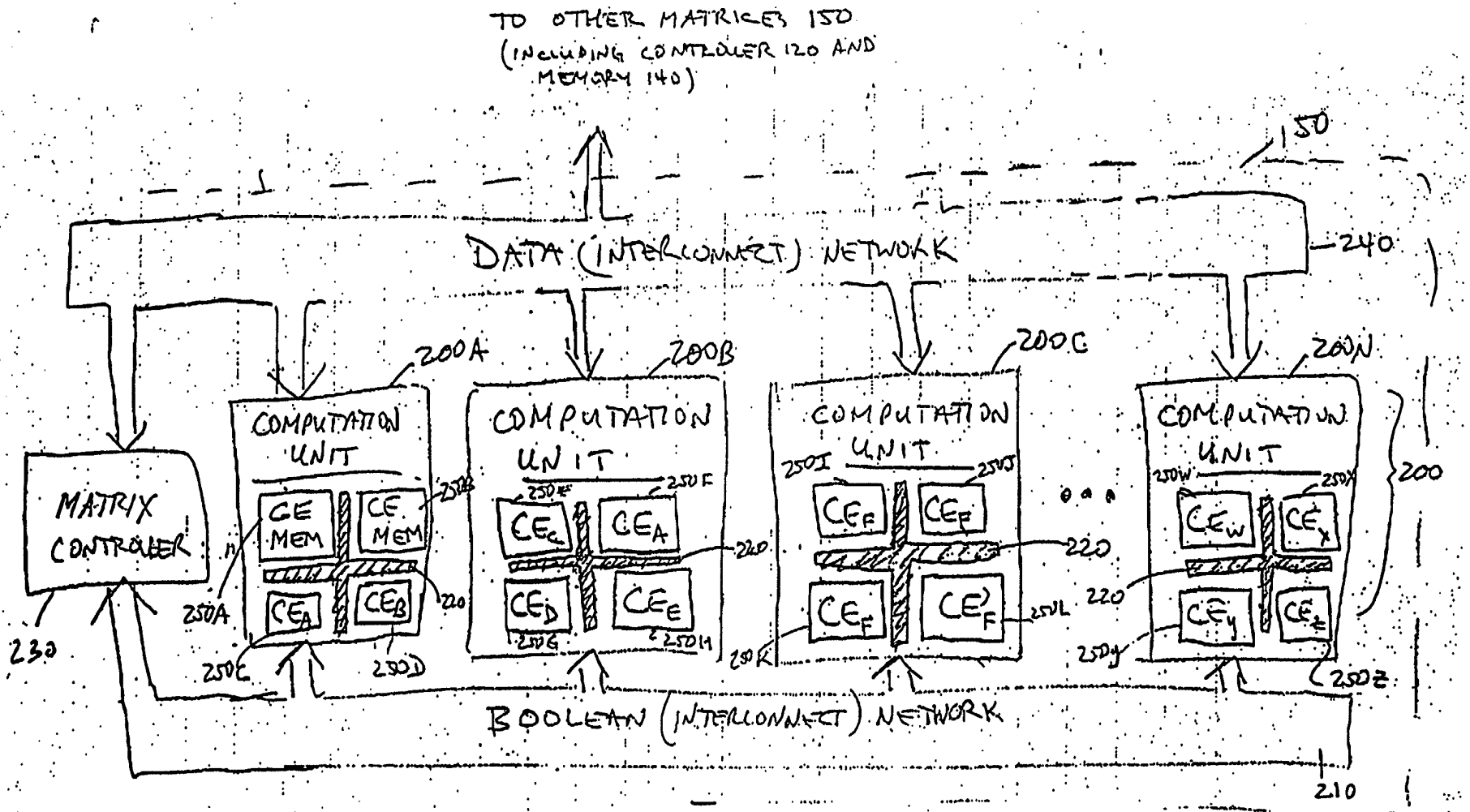


FIG. 3

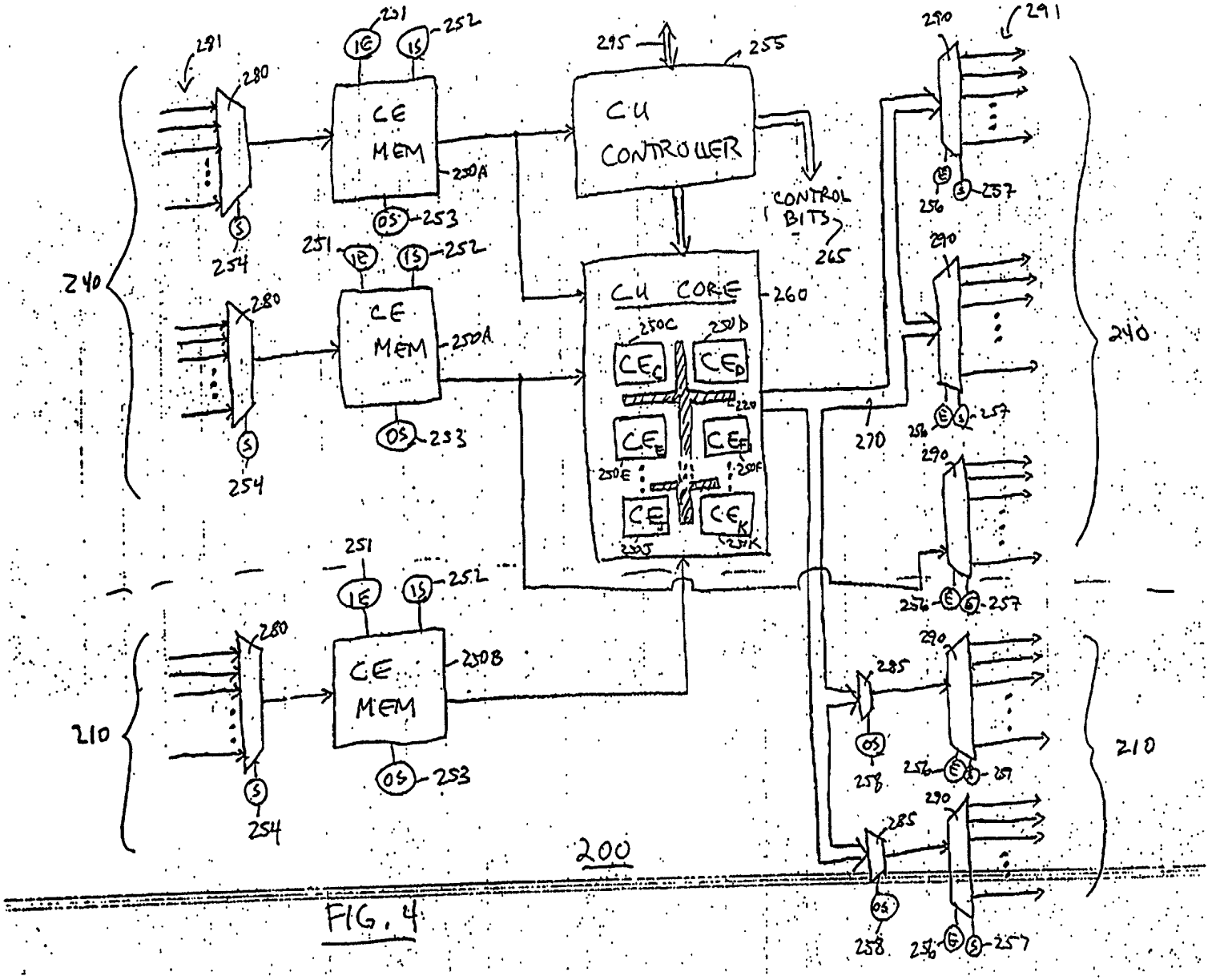

CE MEM
CU CONTROLLER
CU CORE
CONTROL BITS
IE
IS
OS
S
E
240
210
200
270
280
290
291
295
255
260
265
250A
250B
250C
250D
250E
250F
250K
251
252
253
254
256
257
258
285
220

FIG. 4

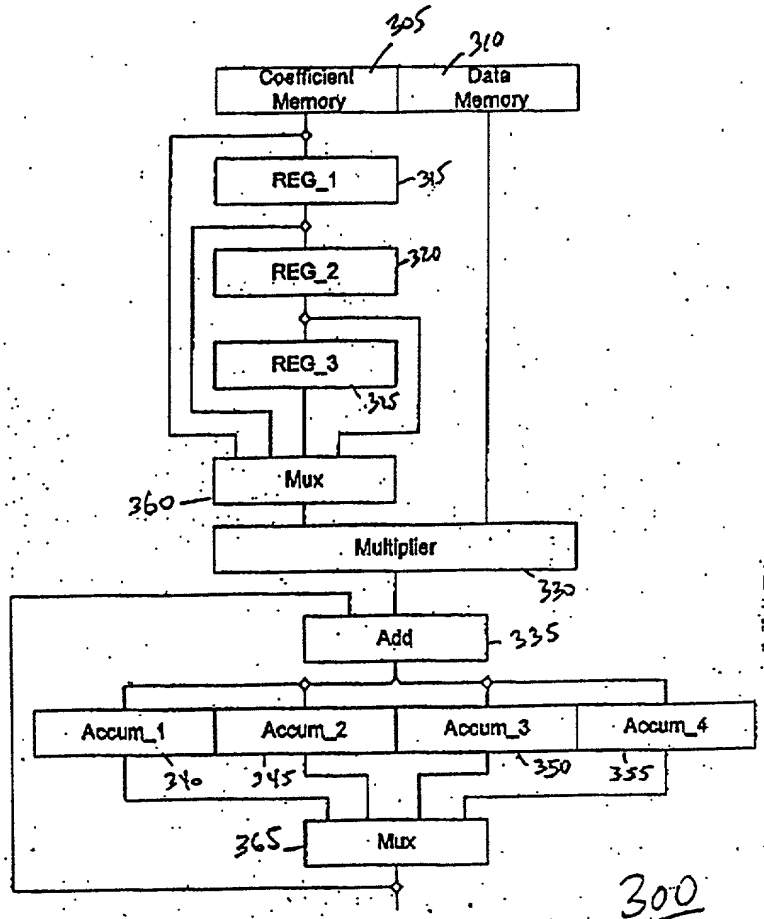

305
310
Coefficient Memory
Data Memory
REG_1
315
REG_2
320
REG_3
325
Mux
360
Multiplier
330
Add
335
Accum_1
Accum_2
Accum_3
Accum_4
340
345
350
355
365
Mux
300

FIG. 5A

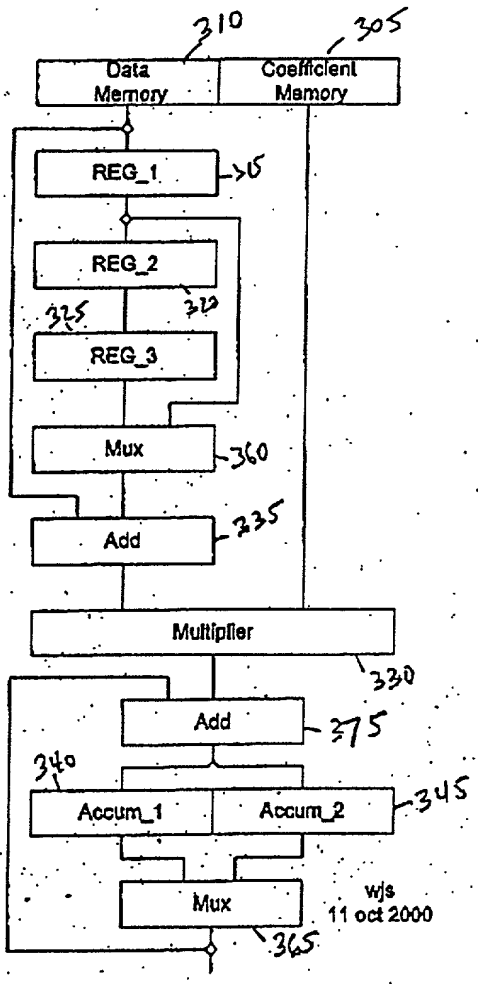
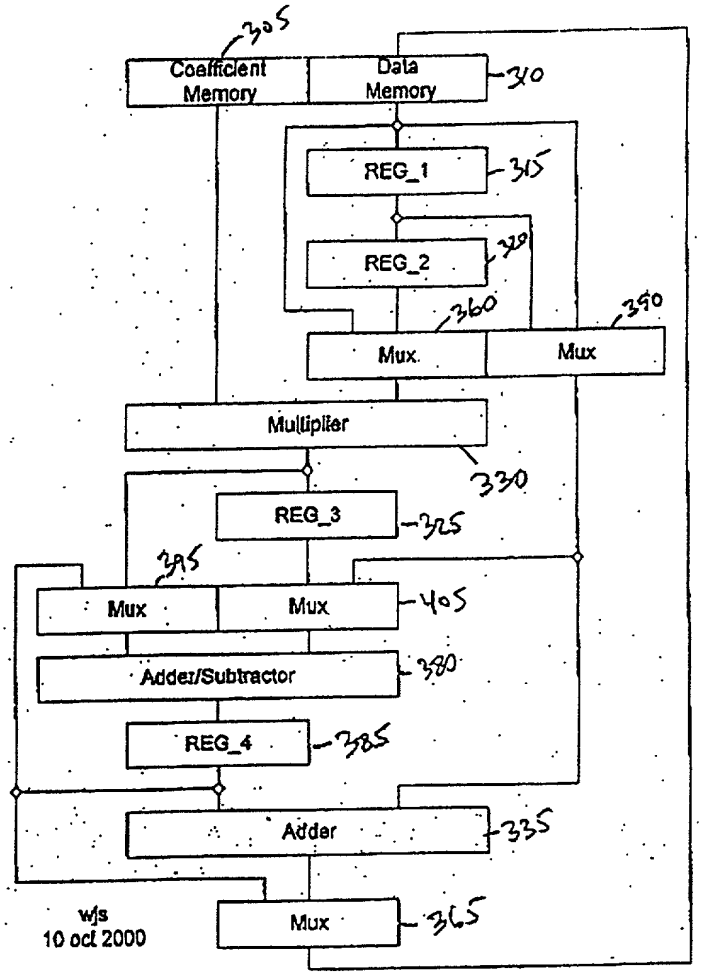
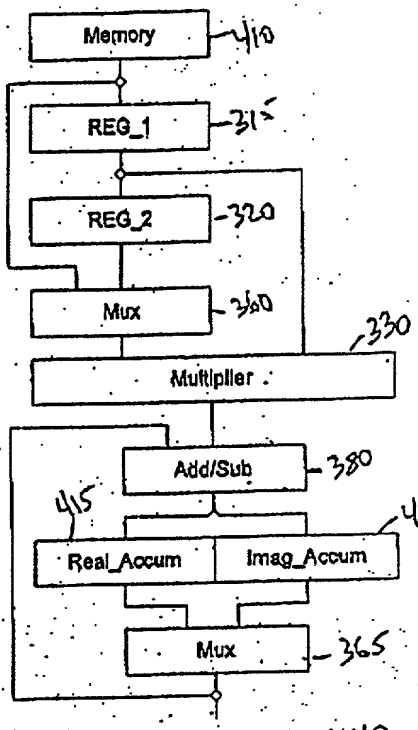

310
305
Data Memory
Coefficient Memory
REG_1
315
REG_2
325
320
REG_3
Mux
360
Add
335
Multiplier
330
Add
375
340
Accum_1
Accum_2
345
Mux
365
w/s
11 oct 2000
370

FIG. 5B


Coefficient Memory
Data Memory
REG_1
REG_2
Mux
Mux
Multiplier
REG_3
Mux
Mux
Adder/Subtractor
REG_4
Adder
Mux
w/s
10 oct 2000

400

FIG. 5C



wjs
19 oct 2000

FIG. 5D

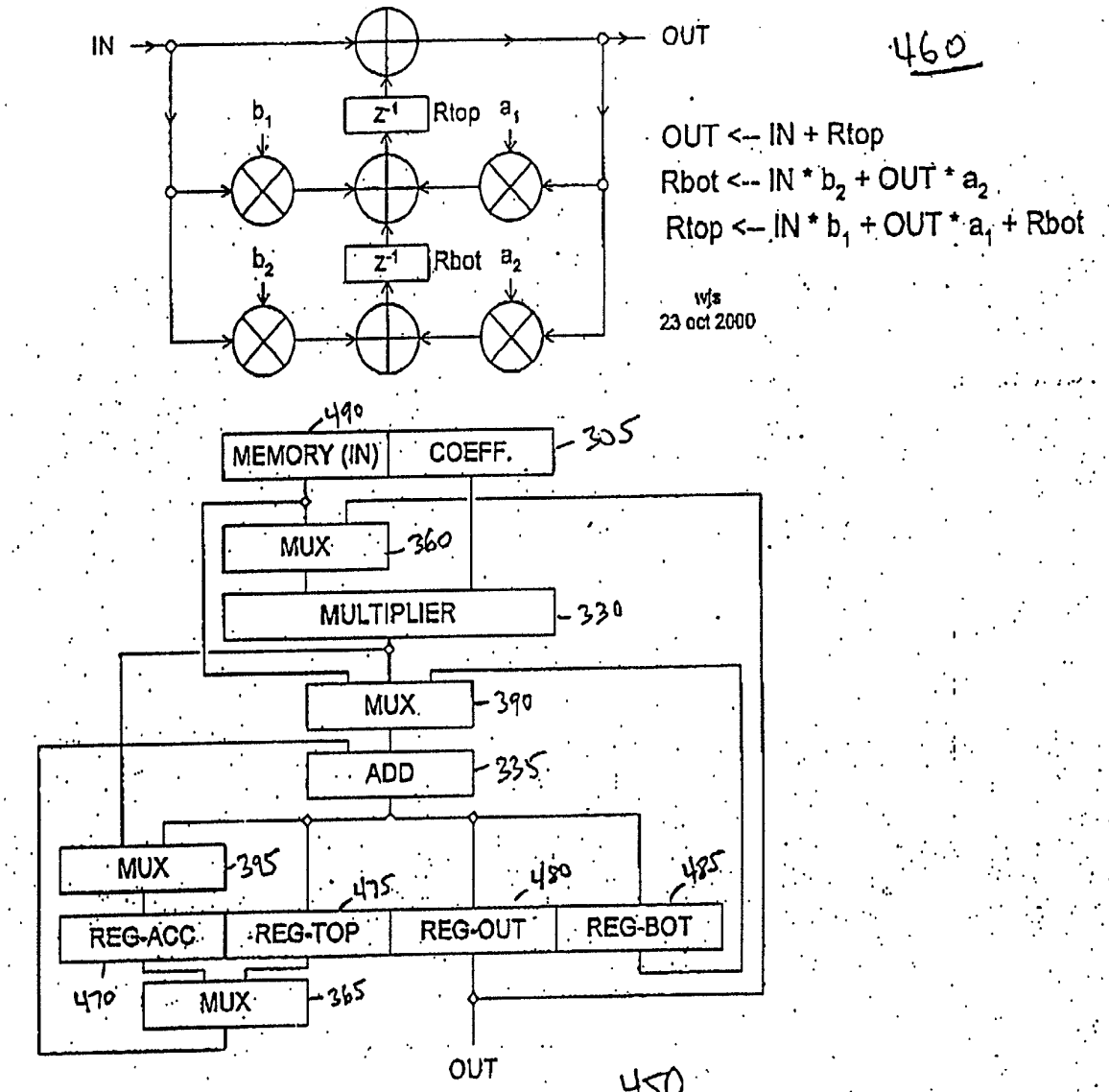

IN
OUT
460
z^{-1}
Rtop
b_1
a_1
b_2
z^{-1}
Rbot
a_2
OUT <-- IN + Rtop
Rbot <-- IN * b_2 + OUT * a_2
Rtop <-- IN * b_1 + OUT * a_1 + Rbot
w/s
23 oct 2000
490
MEMORY (IN)
COEFF.
305
MUX
360
MULTIPLIER
330
MUX
390
ADD
335
MUX
395
475
480
485
REG-ACC
REG-TOP
REG-OUT
REG-BOT
470
MUX
365
OUT
450

FIG. 5E

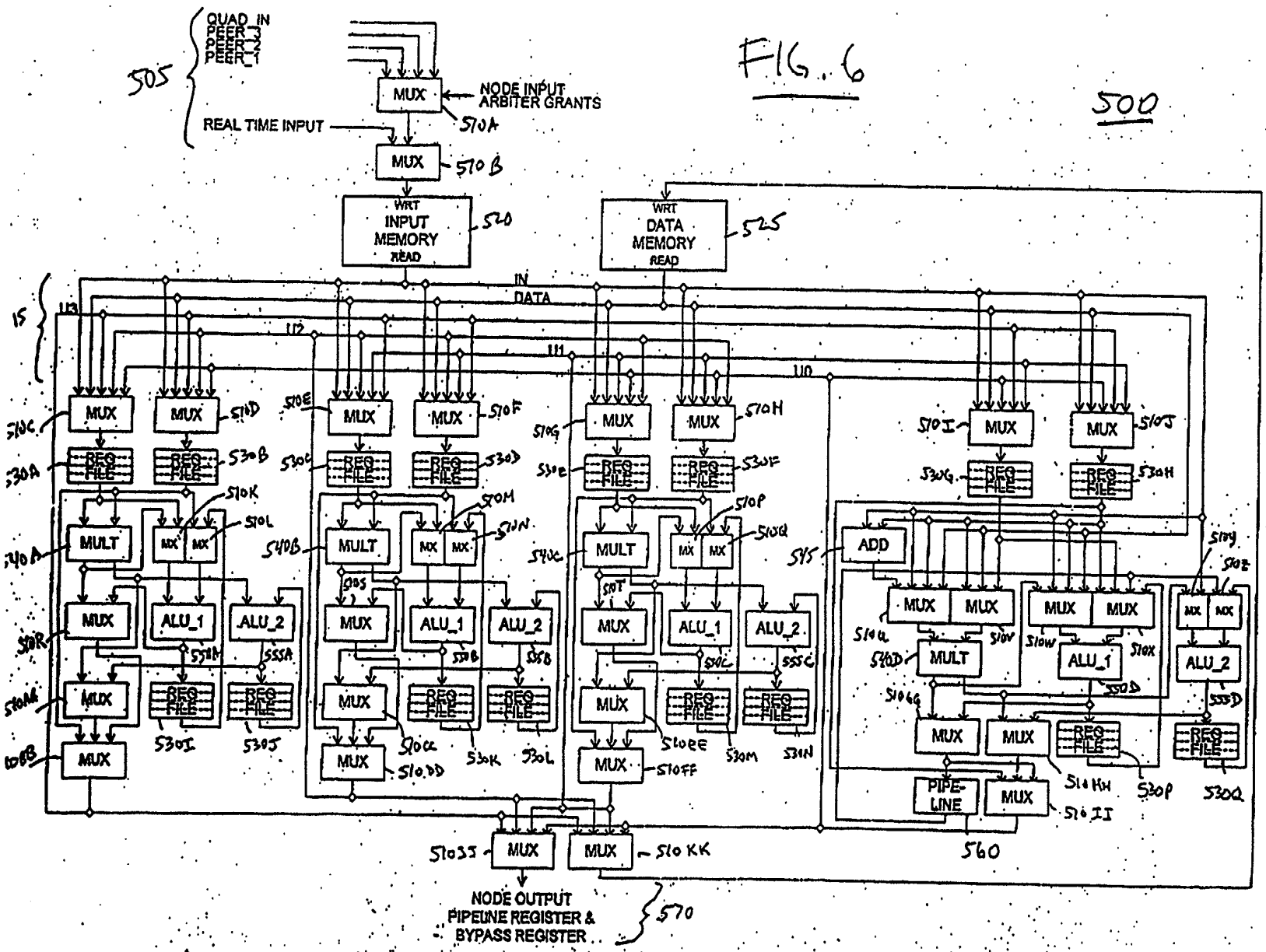


FIG. 6

500

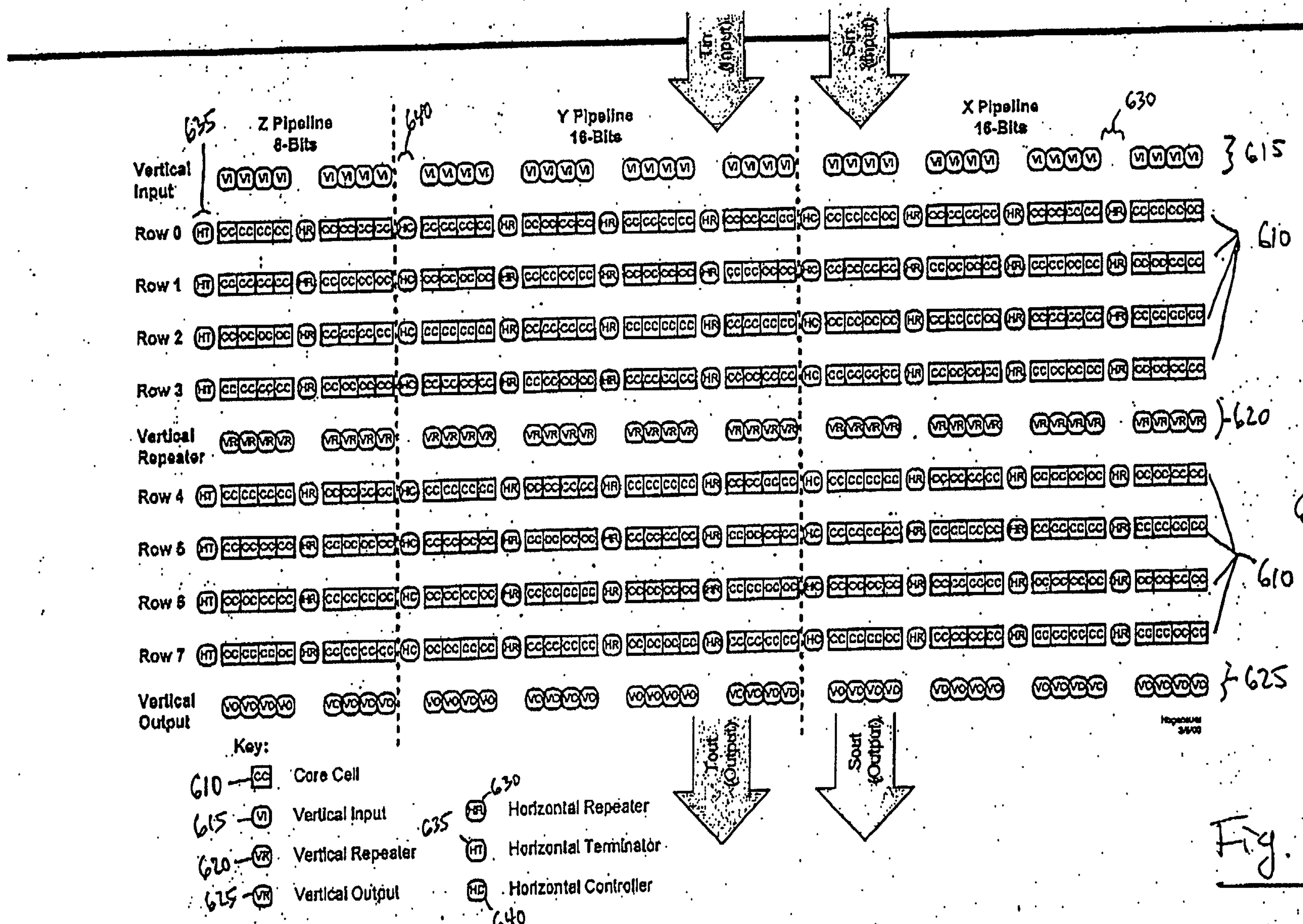

Z Pipeline
8-Bits
Y Pipeline
16-Bits
X Pipeline
16-Bits
Tin (Input)
Sin (Input)
Tout (Output)
Sout (Output)
Vertical Input
Row 0
Row 1
Row 2
Row 3
Vertical Repeater
Row 4
Row 5
Row 6
Row 7
Vertical Output
635
640
630
615
610
620
600
625
Key:
610 CC Core Cell
615 VI Vertical Input
620 VR Vertical Repeater
625 VR Vertical Output
630 HR Horizontal Repeater
635 HT Horizontal Terminator
640 HC Horizontal Controller

Fig. 7

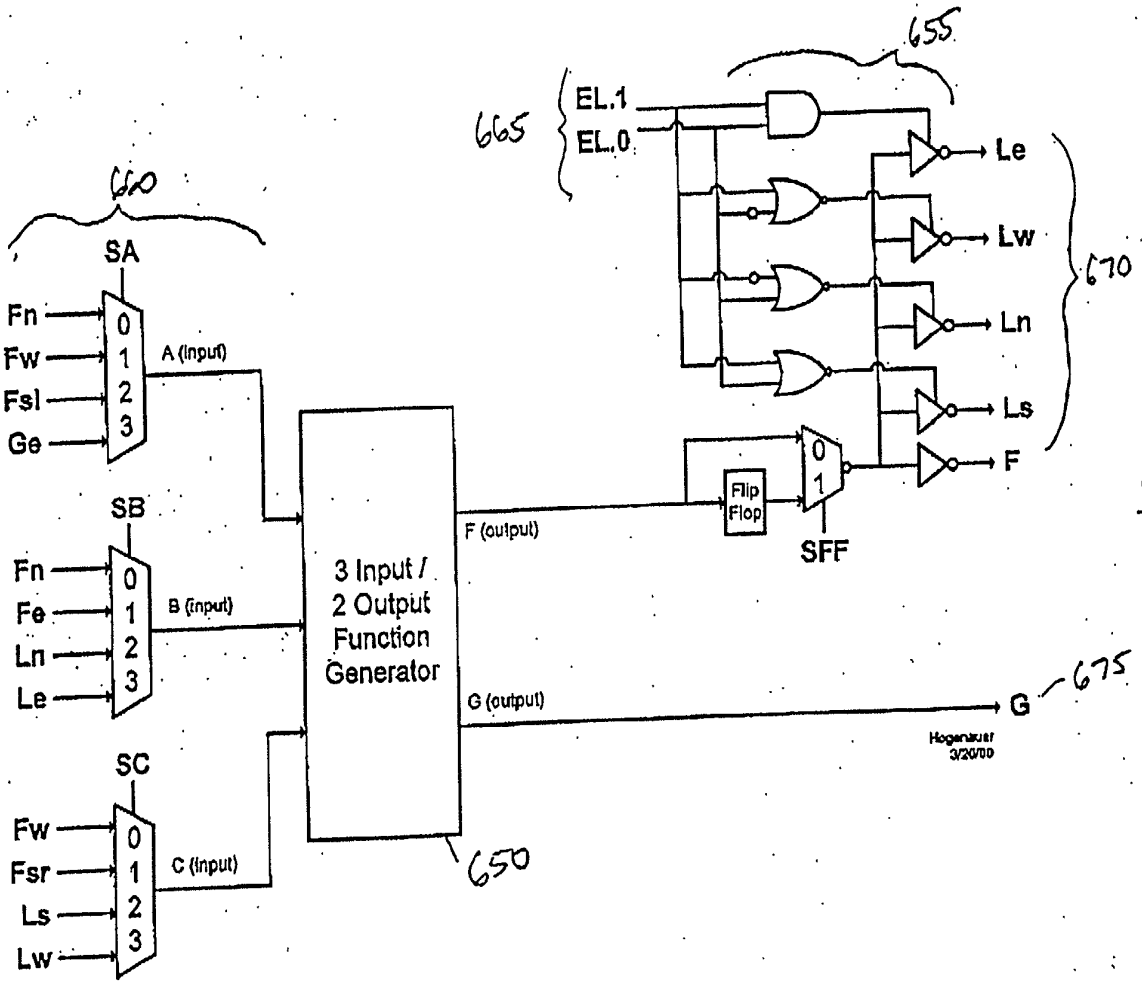

655
665
EL.1
EL.0
660
SA
Fn
Fw
Fsl
Ge
0
1
2
3
A (input)
Le
Lw
Ln
Ls
F
670
Flip Flop
SFF
SB
Fn
Fe
Ln
Le
B (input)
3 Input / 2 Output Function Generator
F (output)
G (output)
G
675
SC
Fw
Fsr
Ls
Lw
C (input)
650
610

Fig. 8

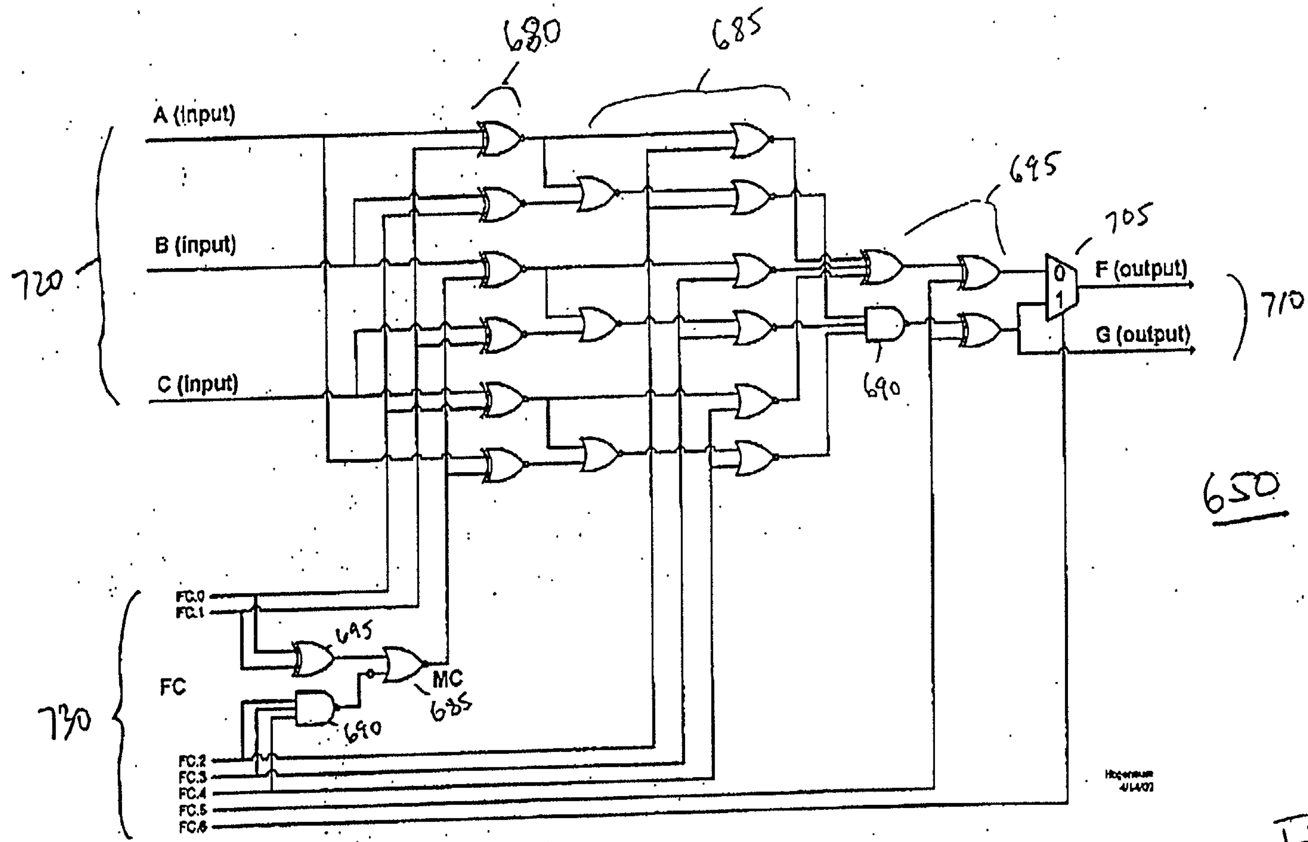


Fig. 9

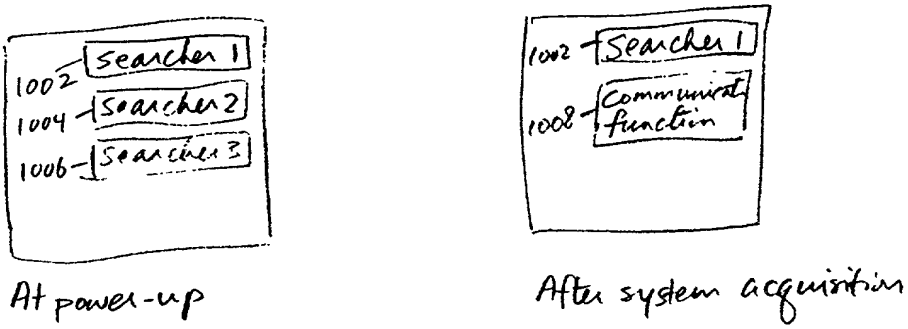

1002
Searcher 1
1004
Searcher 2
1006
Searcher 3
At power-up
1002
Searcher 1
1008
Communicat function
After system acquisition

FIG. 10

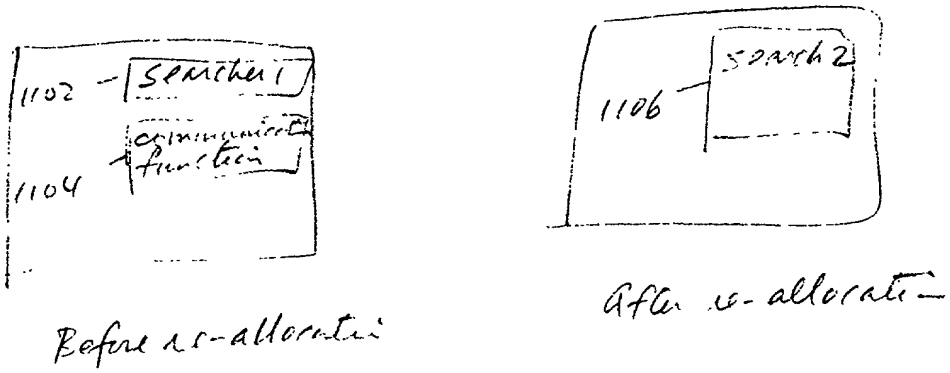

1102
Searcher 1
1104
Search 2
1106
Before re-allocati
Aft re-allocati

FIG. 11

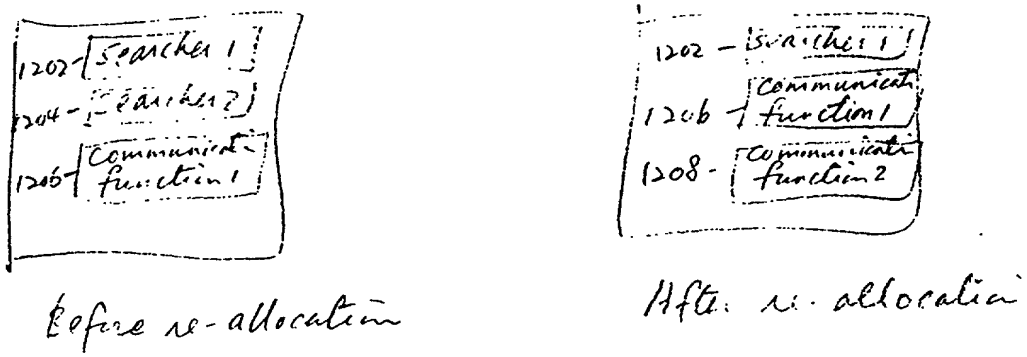

1202
Searcher 1
1204
Searcher 2
1206
Communicati-
function 1
Before re-allocation
1202
Searcher 1
1206
Communicati
function 1
1208
Communicati
function 2
After re-allocation

FIG 12

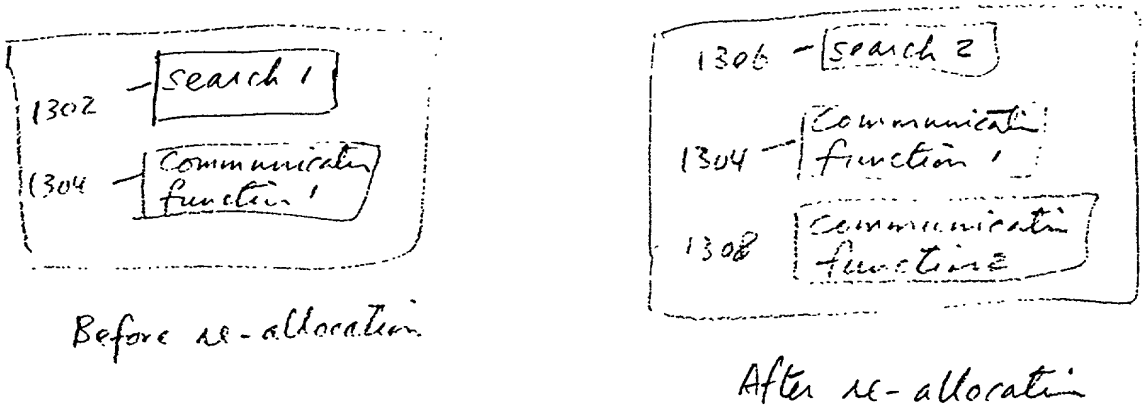

1302
search 1
1304
Communicati
function 1
Before re-allocation
1306
search 2
1304
Communicati
function 1
1308
Communicati
function 2
After re-allocation

FIG. 13